Claim Amendment

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A method for fabricating a semiconductor device structure, the method comprising:

forming a silicon germanium (SiGe) layer on a substrate;

forming a silicon layer on the SiGe layer;

forming a gate oxide layer on the silicon layer;

forming a gate structure on the gate oxide layer;

forming a lightly doped drain region in the silicon layer;

forming a spacer on a sidewall of the gate structure;

performing a doping process on the silicon layer to form a heavily doped drain region beside the lightly doped drain region, and on the gate structure, wherein a dosage of the doping process is about 3E15 to about 5E15 ions/cm^2;

forming a cap layer over the substrate;

performing an annealing process; and

removing the cap layer.

2. (original) The method of claim 1, wherein the doping process is conducted using n-type dopants.

3. (original) The method of claim 1, wherein the doping process is conducted using arsenic ions.

4. (canceled)

5. (original) The method of claim 1, wherein the doping process is conducted with an implant energy of about 60KeV.

6. (original) The method of claim 1, wherein the cap layer is about 300 angstroms to about 700 angstroms thick.

7. (original) The method of claim 1, wherein the cap layer comprises a silicon oxide layer.

8. (original) The method of claim 1, wherein the annealing process is conducted at about 1000 degrees Celsius for about 10 to 20 seconds.

9. (original) The method of claim 1 further comprises forming a silicide layer atop the gate structure and the heavily doped drain region.

10. (original) The method of claim ~~29~~, wherein the silicide layer is selected from the group consisting of tungsten silicide, titanium silicide, nickel silicide, magnesium silicide, platinum silicide and palladium silicide

11. (original) The method of claim 1, wherein the heavily doped drain region is formed in the silicon layer.

12. (original) The method of claim 1, wherein the heavily doped drain region is formed in the silicon layer and the silicon germanium layer.

13. (original) The method of claim 1, wherein the heavily doped drain region is formed in the silicon germanium layer.

14. (original) The method of claim 1, wherein the gate structure is formed with polysilicon or silicon germanium.

15. (original) The method of claim 1, wherein the silicon layer is strained.

16. (currently amended) A fabrication method for a semiconductor structure, the method comprising:

providing a silicon substrate;

forming a gate electrode over the silicon substrate;

introducing n-type dopants to the silicon substrate to form source/drain regions in the substrate beside the gate electrode and to the gate electrode, wherein a dosage of the n-type dopants is about 3E15 ions/cm^2 to about 5E15 ions/cm^2;

forming a cap layer over the doped polysilicon gate;

performing an annealing process; and

removing the cap layer.

17. (original) The method of claim 16, wherein the n-type dopants include arsenic ions.

18. (canceled).

19. (original) The method of claim 16, wherein the annealing process comprises a rapid thermal annealing process conducted at about 1000 degrees Celsius for about 10 to 20 seconds.

20. (original) The method of claim 16, wherein the cap layer is about 300 to about 700 angstroms thick.

21. (original) The method of claim 16, wherein the cap layer comprises a silicon oxide layer deposited at about 400 degrees to 500 degrees Celsius.

22. (original) The method of claim 16, wherein the gate electrode is formed with polysilicon or silicon germanium.

23. (original) A fabrication method for a semiconductor device, the method comprising:

forming a silicon germanium (SiGe) layer on a substrate;

forming a silicon layer on the SiGe layer;

forming a gate oxide layer on the silicon layer;

forming a gate structure on the gate oxide layer;

implanting arsenic ions to the strained silicon layer to form a lightly doped drain region;

forming a spacer on a sidewall of the gate;

implanting arsenic ions to the strained silicon layer and a top surface of the silicon germanium layer to form a heavily doped drain region beside the lightly doped drain region and to the gate structure;

forming a cap layer over the substrate;

performing a rapid thermal annealing process;

removing the cap layer;

forming a nickel silicide layer atop the gate structure and the heavily doped drain region.

24. (original) The method of claim 23, wherein the gate structure is formed with polysilicon or silicon germanium.

25. (original) The method of claim 23, wherein a dosage used implanting the arsenic ions to the strained silicon layer and a top surface of the silicon germanium layer, and to the gate structure is about 3E15 to about 5E15 ions/cm^2.